# **Ultrasonic Sensor Project for Senior Design**

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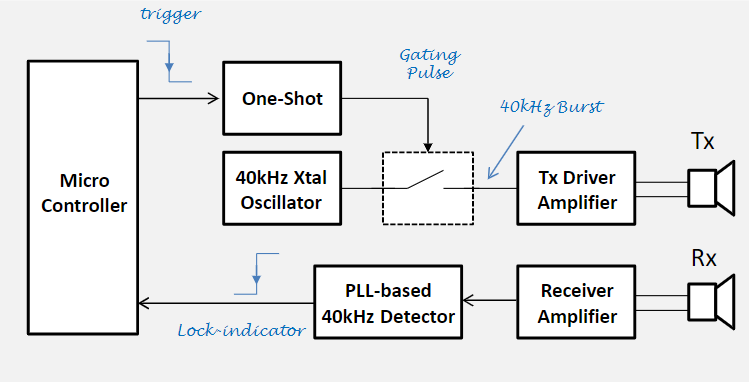
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**Abstract**

*This paper goes through the development of the ultrasonic sensor from the ground up using mostly off-the-shelf products as a formalized design exercise supervised by Professor Steve Dunton for EE449. This paper covers the significance of each submodule to the design and the non-idealities that created the changes in what was created as the final product.*

1. **Layout & Submodules**



**Figure 1. General Layout of the Ultrasonic Sensor**

A. *Transmitting Circuit*

The transducers emit a 40kHz signal and utilize the time between two narrow 40kHz pulses (transmitted and received pulse) or ‘chirps’ to determine the distance from the sensors. An ECS-31x [1] crystal oscillator is used to construct the Pierce crystal oscillator that sends 40kHz to a CD4066B CMOS [6] quad bilateral switch that is activated from a microcontroller through the one-shot circuit, sending a 40kHz pulse to the TC4428A MOSFET [2] gate driver that drives the transmitting transducer (TX).

B. *Receiving Circuit*

For the receiving transducer (RX), a LM567x [8] PLL-based tone decoder is used to discern the 40kHz ‘chirp’ from environmental noise and then output an active low signal that signifies the detected sound to our Arduino Uno. This is still a very simplified

explanation of the project as many modifications were made to achieve the ultrasonic sensor’s ability to calculate distances up to 3.5m.

C. *Core Design Specification*

The sole requirement and specification for this project at a high level remains: achieve proper calculation of distances from the ultrasonic sensor up to, or more than, 3.5m.

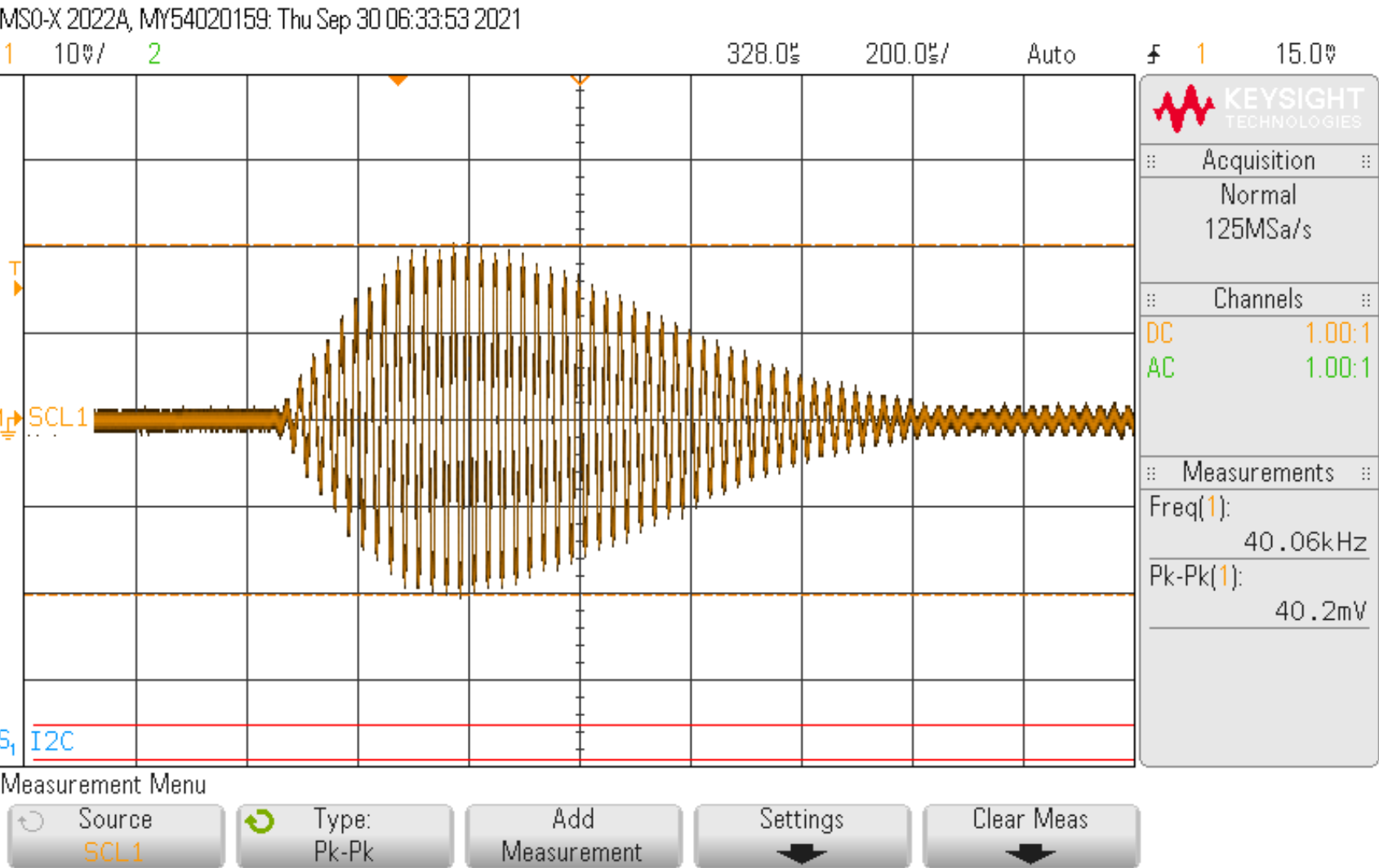
1. **Transducers**

A. *Transducer Performance in Frequency Domain*

The transducers’ individual frequency responses were determined from their joint frequency response (each supplied by 9V DC power), as their joint frequency response would be used to understand the functional bandwidth and resonant frequency of their use in our circuit.

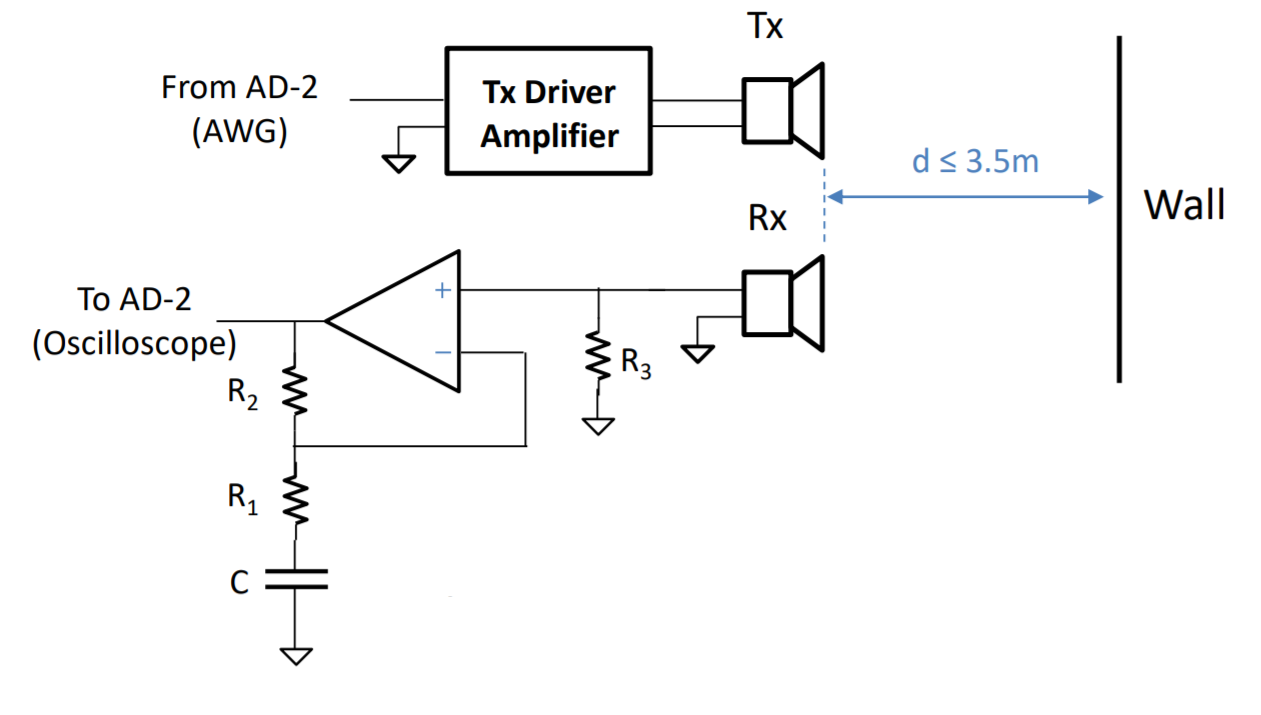
After incrementally measuring the magnitude of each transducer in steps of 50Hz (using a Keysight signal generator) on the Keysight MSOX2022A, the excel solver tool calculated a resonant frequency for the TX as 39.308kHz and the RX as 40.244kHz, resulting in a joint resonant frequency of 39.776kHz.

To test the functionality of the transducers’ ability to transmit 40kHz chirps, we sent a ~5V DC pulse to the TX, which the RX would receive as a ~20mV 40kHz step response.



**Figure 2. Recorded 40kHz RX Step Response**

B. *RX Amplification Design*



**Figure 3. Initial RX Amplifier Design**

The passive component values of this amplifier to achieve the transfer function’s gain in decibels were determined by a Matlab program I wrote. Aiming for 40dB gain, it was determined that 60dB worked better at farther distances while 20dB gain worked at closer distances. The following values were used to achieve our 45dB gain:

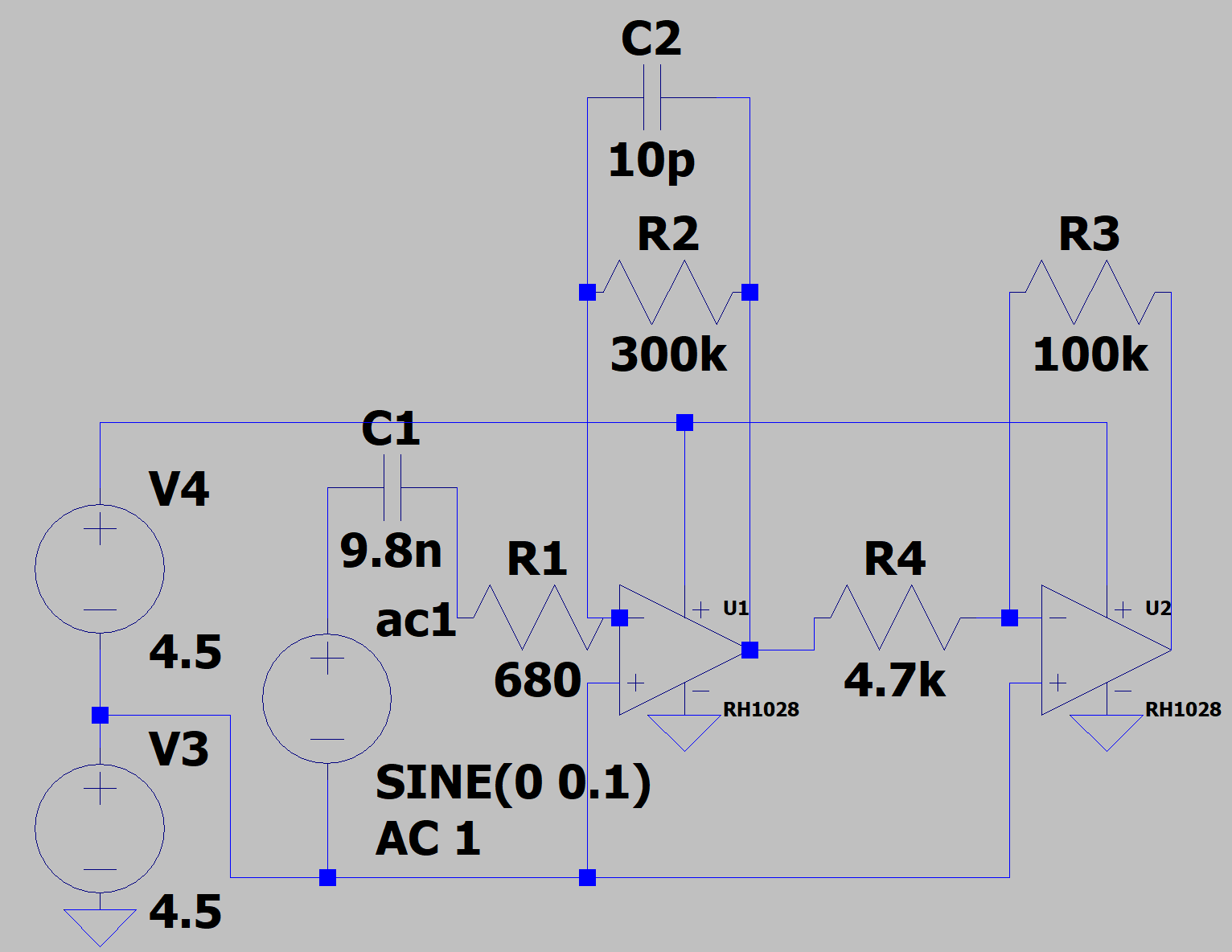
R1: 1.2kΩ R2: 220kΩ

R3: 1MΩ C: 100nF

C. *Modified Amplifier Circuit*

After a linearized forecasting model of our transducers’ limits, it was determined that the single-stage gain setup would only be able to reach 1.5m (realistically) and 2m at best. The 1-stage op amp would not be able to achieve the 3.5m detection requirement. The 2-stage op amp is now used in series with an active filter to get a seemingly innocent 20dB gain that delivered rail-to-rail 40kHz signal detection for the RX transducer consistently.

With the LMC662 [9], the two op amps inside were used to create a two-stage gain in the following figure.



**Figure 4. Two-Stage Op. Amp. for RX Amplification**

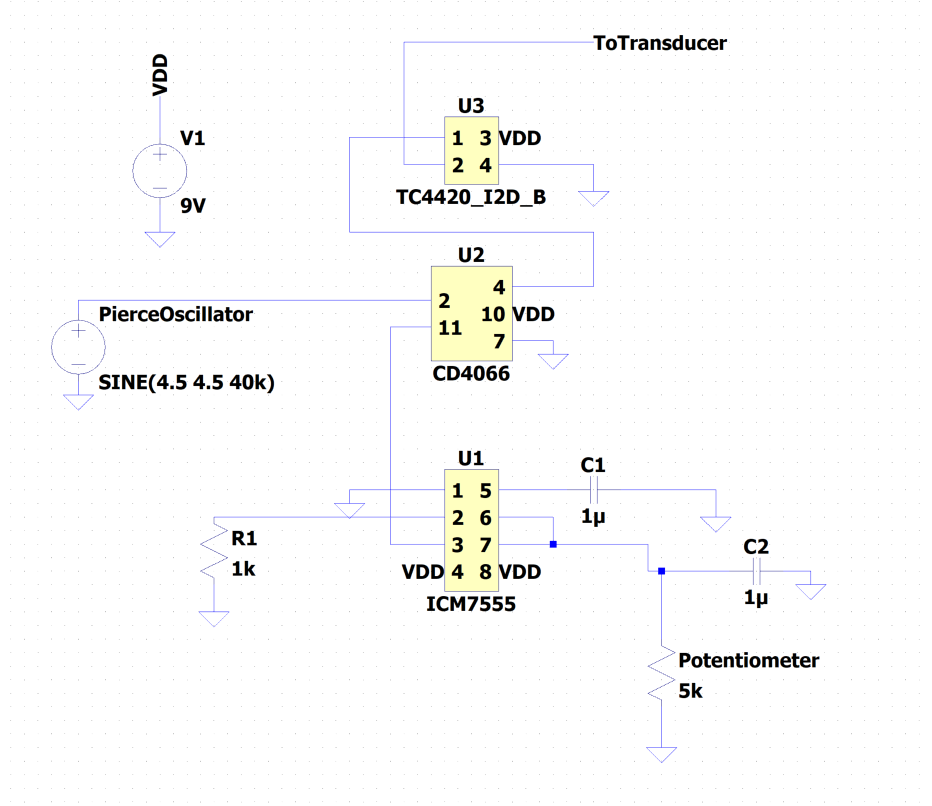
*D. Active Filter Design*

The design of these two gain stages from the LMC662CM [9] op amps serves a dual purpose as the first stage adds gain to the signal and acts as an active bandpass filter at around a 10kHz bandwidth centered around 40kHz resonant frequency to reduce the detectable environmental noise of the EE lab.

These two stages together create 20dB gain and allow for a rail-to-rail signal on the RX transducer’s end, making a more discernible ‘chirp’ that can determine the distance from the ultrasonic sensor better.

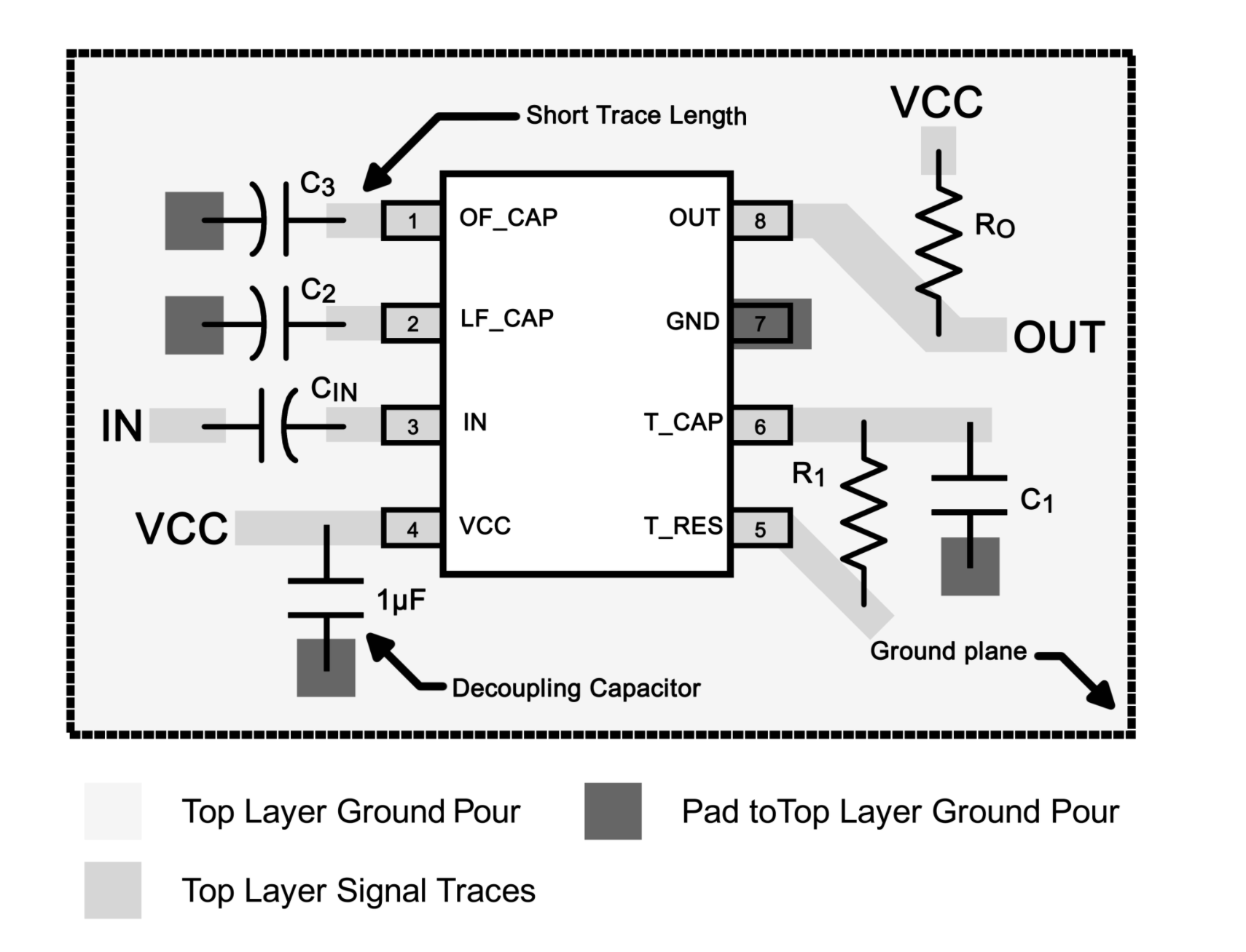
**III. One-Shot & Gate Driver**

A 1ms trigger from the Arduino Uno triggers the 5ms signal from the ICM7555 [10] to allow the switch to let the 40kHz signal through to the TC4426A [2] gate driver to power the oscillating signal into the transmitting transducer as demonstrated in the figure below.



**Figure 5. One-Shot Gate Driver Design**

**IV. PLL-Based Tone Decoder**

The LM567x [8] has a very specific set up to bias the circuitry inside to allow the submodule to detect 40kHz. 

**Figure 6. LM567x Setup Used for PLL-based Tone Decoder**

100nF was used for C2, 300nF was used for C3, 2.75kΩ was used for R1, 4.7kΩ was arbitrarily chosen for Ro, and 100nF was used for Cin.

The equation below is what is used to calculate the resonant frequency according to TI’s data sheet.

(1)

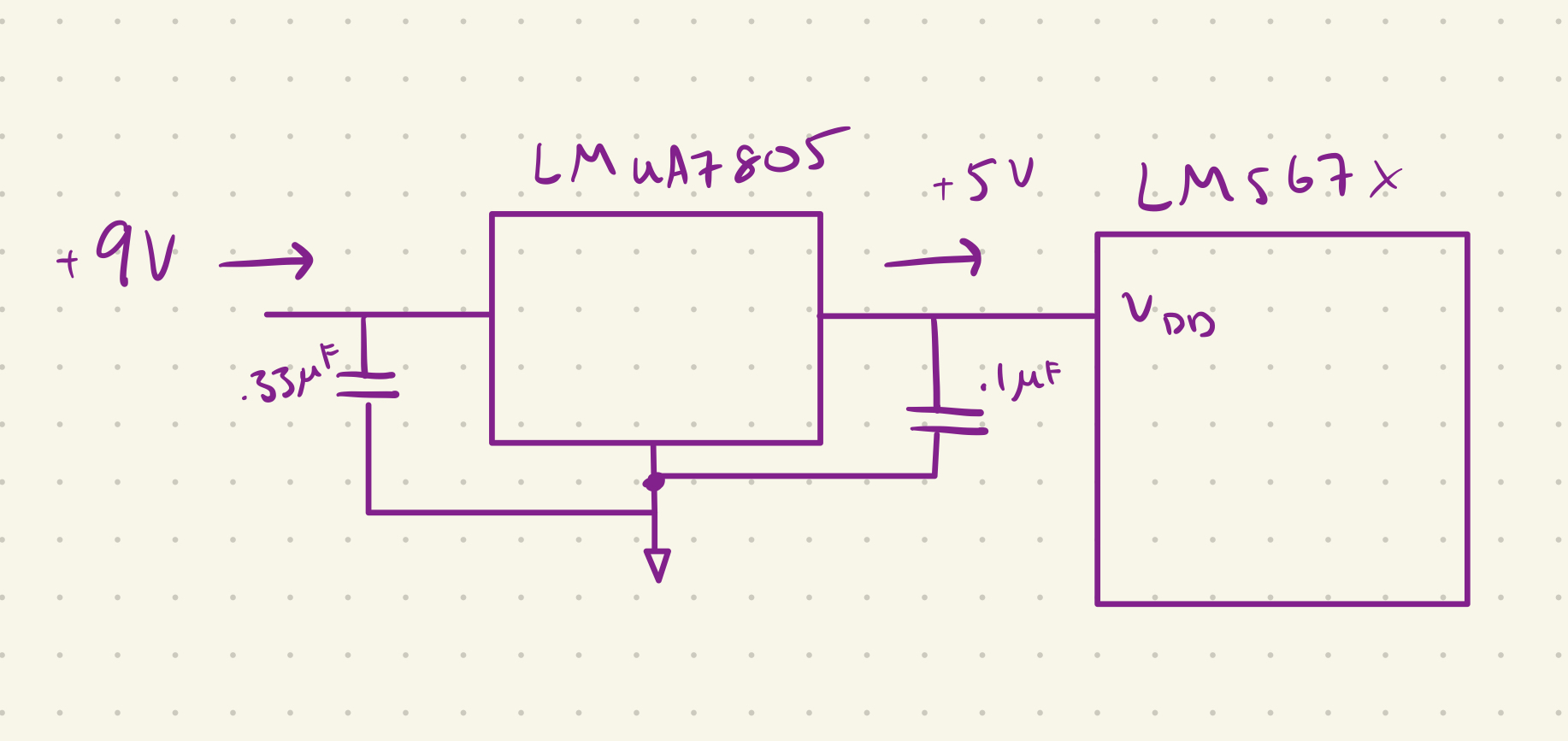
According to TI, the C3 capacitor ought to be at least two times greater than that of C2 for the output filter to work. At less than 200mV input voltage, the bandwidth of the tone decoder changes as a percent of the resonant frequency as described in equation 2.

(2)

The LM567 module [8] offered incredible difficulty when it came to operating at the minimum input voltage of 20mV. The bandwidth of the recognizable resonant frequency changed drastically depending on the amplitude of the input signal. This led to a great investigation into both the PLL inside and the two-stage amplifier at the input.

After consulting Professor Dunton and iteratively trouble shooting all possible components and sub module functionalities, I thought the LM567 [8] might be giving us trouble. Even with perfected input amplifiers producing a clean input at varying frequencies, the LM567 [8] offered varying performance simply by moving up or down in frequency.

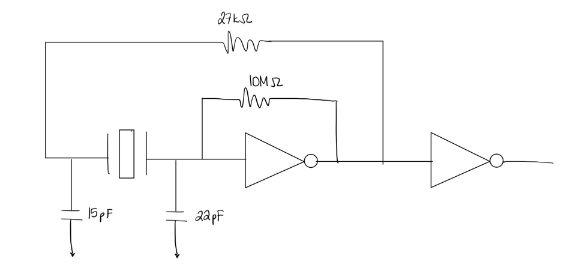
This was solved after realizing other groups were using split rail power supply levels for the LM567 [8] from -4.5V to 4.5V instead of 0 to 9V. After supplying the PLL’s power rail with 0 to 5V, the tone decoder was able to cleanly catch onto the 40kHz signal after varying frequencies.



**Figure 7. LM7805 Voltage Regulator to PLL [4]**

It’s not clear as to why the LM567 [8] can’t seem to lock on at higher voltage supply, but a 5V supply rail seems to work best.

**V. Pierce Crystal Oscillator**

The Pierce Crystal Oscillator uses the ECS-31x [1] as its core component. With a perilous four weeks of issues, the out-of-phase system was corrected by changing the ground of the capacitors from a relative kind of floating ground to a common ground. 

**Figure 8. Pierce Crystal Oscillator Configuration**

The system takes ambient EM noise from the environment and amplifies it into a self-stabilizing input signal that has matching 360 degrees phase difference between the input and output signal due to the first inverter providing 180 degrees, and the rest of the system providing the remaining phase shift (aside from the final inverter).

The Pierce crystal oscillator using the EC-31s [1] was incredibly difficult to construct for a while as the capacitors were being attached to a virtual ground and not the actual ground, leading to a seemingly impossible to work crystal oscillator.

To speed up the amplification of ambient noise, coiled banana cable was used as the noise input antenna briefly to amplify the ambient EM noise faster into the oscillating system.

**VI. Finalization of Design**

A considerable amount of effort went into looking for a solution to high frequency RFI noise for a little while as 100kHz+ noise plagued and saturated our amplifiers and tone decoder. This was adjusted by running it off a battery with a very large capacitor coupling the power supply and ground rail temporarily as an experiment.

Reconstruction of many submodules have adjusted the amount of RFI noise our system conducted, but the battery-powered supply rail helped temporarily before the RFI noise resumed.

**VII. Last Words**

This project was quite difficult in the randomness of the problems we had to address. It was thoroughly deliberated over as to how this board gave us such headaches and pains despite the submodules working splendidly on their own. Sifting through power requirements and working longer weekend hours to get millimeters closer to figuring out what plagued our system was arduous.

It’s still not determined as to what exactly has given us such blocks to our progress, but to our peers and supervising Professor, it eludes them as well.

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